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Applicant(s)	John E. Donohue	
Serial NoFEB 2 4 2003	09/432,022	AMENDMENT
Filing Date Group Art Unit	October 29, 1999	AND RESPONSE
Group Art Unit	2631	<u>UNDER 37 C.F.R. § 1.111</u>
Examiner Name	Pankaj Kumar	3
Confirmation Number	9521	
Attorney Docket No.	100.116US01	
Title: SYSTEMS AND METHODS FOR HOLDOVER CIRCUITS IN PHASE LOCKED		

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Commissioner for Patents Washington, D.C. 20231

Applicants have reviewed the Office Action mailed on November 15, 2002. Please amend the above-identified application as follows.

ABSTRACT

Please amend the Abstract to read as follows:

Improved phase locked loops are described which handle momentary breaks in an input communication channel. The phase locked loops provide the capability to "hold" the output clock in a communication system at or very near the last output frequency before the loss of input data. Such phase locked loops include a differential phase detector, an electronic selector circuit, and an operational amplifier based loop filter circuit. The electronic selector circuit provides the differential output of the phase detector at a pair of inputs to the operational amplifier. A voltage controlled oscillator is coupled to an output of the operational amplifier and provides an output frequency for the phased locked loop circuit. The electronic selector circuit is operable to control the input to the operational amplifier to hold an output frequency of the voltage controlled oscillator at a substantially constant frequency.

